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DEVELOPMENT OF A CCD ARRAY AS AN IMAGING DETECTOR FOR
ADVANCED X-RAY ASTROPHYSICS FACILITIES

NASA Grant NSG-7615

Final Report

For the Period 1 June 1979 to 31 January 1981

Principal Investigator

Daniel A. Schwartz

April 1981

Prepared for
National Aeronautics and Space Administration
Washington, D.C. 20546

Smithsonian Institution
Astrophysical Observatory
Cambridge, Massachusetts 02138



The Smithsonian Astrophysical Observatory
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The NASA Technical Officer for this grant is Dr. Albert G. Opp,
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TABLE OF CONTENTS

	<u>Page</u>
1.0 INTRODUCTION	1
1.1 Objectives	1
1.2 Investigation	4
1.3 Summary and Conclusions	7
2.0 SPECIFIC ACCOMPLISHMENTS	10
2.1 Study of Available Chips	10
2.2 CCD Camera	13
2.3 CCD Mounting and Cooling	16
2.4 System Analysis and Rework	19
2.4.1 Cooling	19
2.4.2 System Noise	21
2.5 Performance	25
2.5.1 Functional	25
2.5.2 X-ray Results	28
2.6 Westinghouse Subcontract	34
2.7 Camera System for Westinghouse Chips	39
2.7.1 Microprocessor System	39
2.7.2 Analysis and Control Computer System	44
2.7.3 Initial Operation	50
3.0 PUBLICATIONS	53
4.0 REFERENCES	54

TABLE OF FIGURES

	<u>Page</u>
1. Schematic of CCD operation	2
2. Theoretical energy resolution	3
3. Fairchild 211 system	14
4. Optical illumination of 211	17
5. CCD vacuum mount	18
6. CCD analog processing	23
7. Response of 211 to X-rays	29/30
8. X-ray image from 211	33
9. Charge transfer in Westinghouse linear array	36
10. Backside illumination of Westinghouse linear array	38
11. Microprocessor configuration	40
12. Microprocessor software system	42
13. X-ray CCD computer hardware	45
14. NOVA software functions	46
15. NOVA analysis software	48
16. Operation of Westinghouse area array	52

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1.0 INTRODUCTION

1.1 Objectives

Charge Coupled Devices (CCDs) promise great benefits for X-ray astronomy. They provide high spatial, and therefore high angular, resolution because their geometric construction traps charge within pixels of about $20\mu\text{m}$ size (Figure 1). The atomic number of silicon, $Z = 14$, makes it ideal for stopping X-rays up to 10 keV, limited at lower energies to above 1/4 to 1 keV for reasons discussed below. The mean conversion efficiency of 3.6 eV per electron-hole pair, together with the low Fano factor, $F \approx 0.12$, theoretically allows an accurate determination of the energy of each incident X-ray. A full-width-half-maximum (FWHM) resolution of 150 to 400 eV should be attainable depending only on the system electronic noise (Figure 2).

Use of a CCD X-ray Imager on a large aperture, high angular resolution X-ray telescope will allow qualitatively new scientific observations which would simply be too expensive in observing time to carry out by detectors presently available. The Advanced X-ray Astrophysics Facility (AXAF) currently under

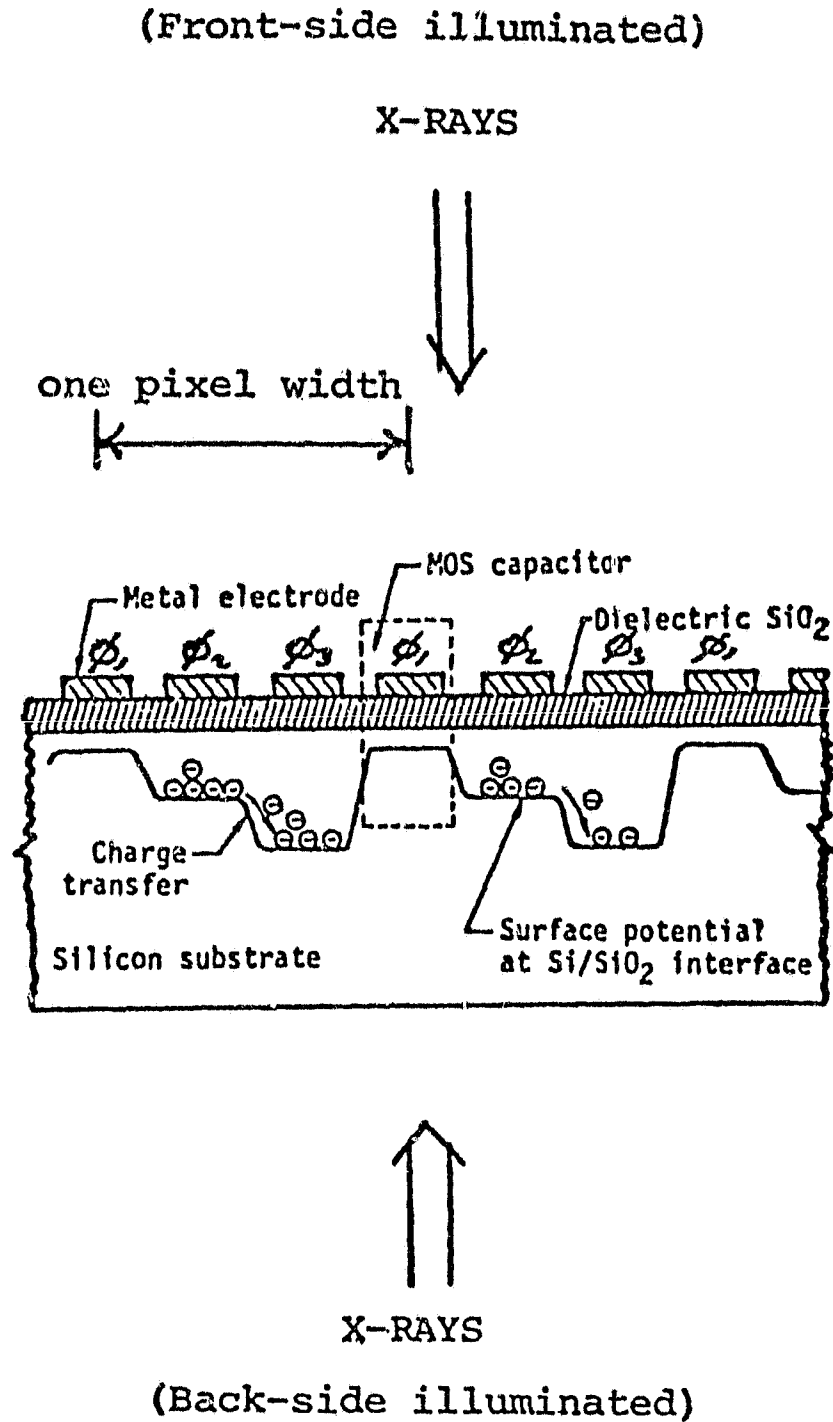


Figure 1. Schematic of CCD operation. A 3-phase device is shown.

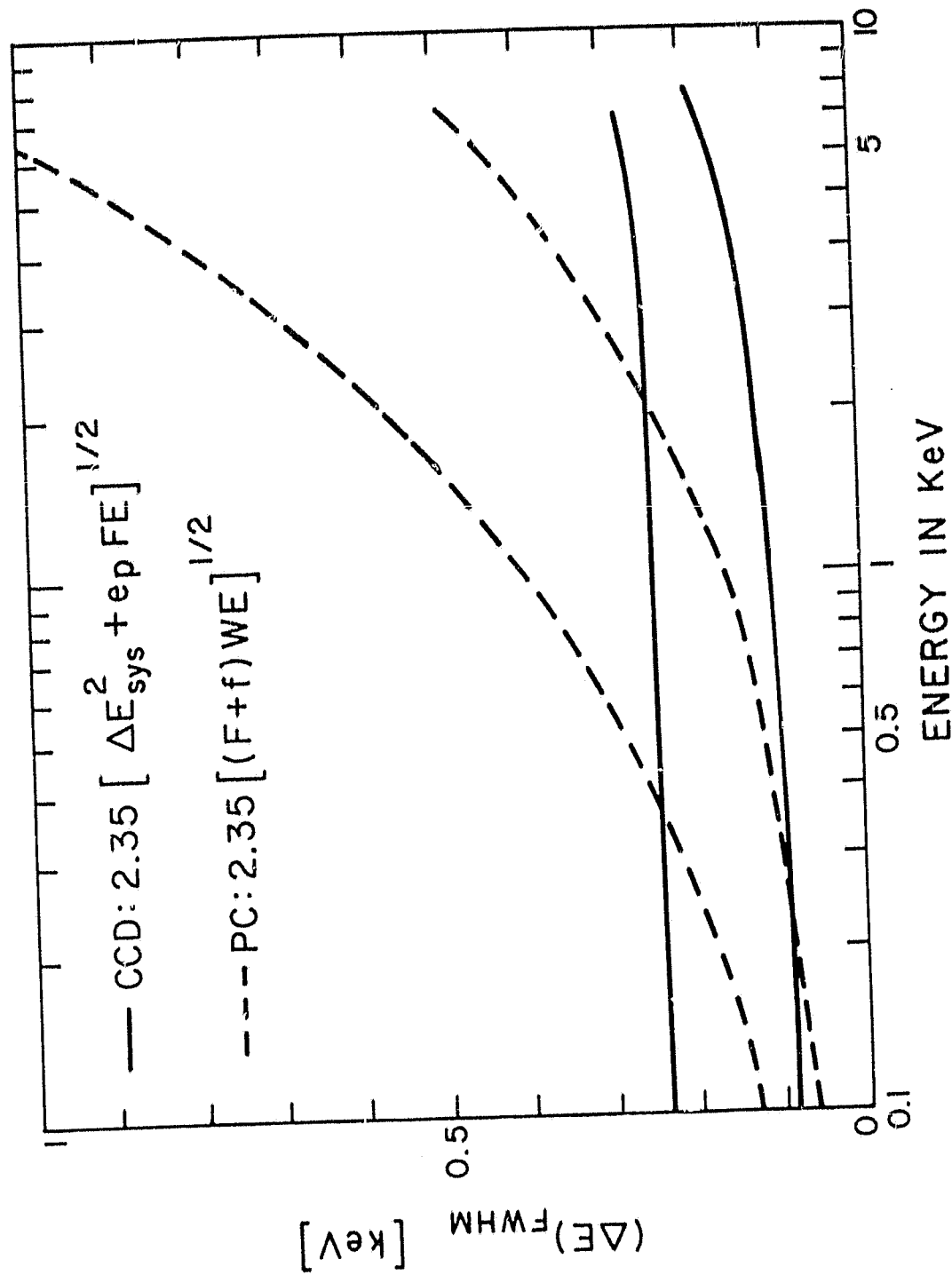


Figure 2. Theoretically attainable energy resolutions from an imaging CCD (solid lines), or from non-imaging versions of a proportional counter (upper dashed curve) or a gas scintillation proportional counter (lower dashed curve). The system noise $(\Delta E)_{sys}$ is assumed to be e_p times 10 or 30 electrons rms for the two CCD curves. The Fano factor is F , the gas gain variation factor is f , and $e_p = 3.6$ eV/electron hole pair in Silicon or $W = 30$ eV/ion pair in Argon represent the conversion factors.

study [1,2,3] would provide a suitable telescope, along with necessary support facilities such as a celestial aspect system, power and telemetry. Even considering only the high angular resolution and high quantum efficiency, a CCD theoretically allows the highest possible detection sensitivity for deep surveys and for features of low surface brightness contrast, within its energy range. In addition, there is a large class of experiments where it is desirable to measure X-ray spectra resolved spatially into 1-10 arcsec elements. These include studies of the distribution of iron and silicon in clusters of galaxies, measurements of temperature and abundance gradients in supernova shock fronts, distinguishing the central point source, halo, and jet seen in Centaurus A, and enabling spectral studies of the individual point and diffuse sources in irregular clusters of galaxies, Perseus/NGC 1275, Orion, Eta Carina, and the M31 nucleus.

The purpose of the present investigation was to obtain laboratory data showing the extent to which CCDs can perform up to expectations. Specifically, can we detect single, localized X-ray interactions? What is the quantum efficiency and energy resolution as a function of X-ray energy? How well can a CCD be incorporated into a space flight instrument?

1.2 Investigation

Through our previous work [4] we had identified some

potential difficulties regarding the performance of CCDs. These occur in the area of quantum efficiency, energy resolution, and format. The implication is that a given CCD system must be chosen for specific scientific objectives. (A corollary is that different CCD systems might be used for various X-ray astronomy missions.) Our present study only concerns the application of a CCD as a general purpose, high resolution imager on AXAF.

Low energy quantum efficiency is cut-off below about 1 keV for front-side illuminated devices due to absorption in the "gate" electrode structures (see Figure 1), typically a 1 to 2 μm layer of Si or SiO. For back-side illumination however, a passivation layer of no more than 0.1 to 0.5 μm would allow useful response down to 1/4 to 1/2 keV. In a conventional back-side illuminated device, the CCD substrate is thinned to about 10 μm , so that the quantum efficiency for the 6.7 keV Fe-line X-rays is reduced significantly (to less than 20%). For a conventional front-side illuminated CCD, the high energy X-rays all stop within the thick silicon substrate, but only the fraction (typically less than 75% [5]) for which charge-carriers can diffuse up to the depletion layer (typically 5 μm thick) before recombination, register as X-ray events.

This same diffusion and loss of charge-carriers in a CCD with a conventional depletion depth causes a degradation of energy resolution above about 4 keV for front-illuminated

devices, and at all energies for back-illuminated devices. There are three regimes: 1) All charge collected in a single pixel; 2) All charge collected, but spread among several adjacent pixels; 3) Some charge lost to recombination, and the remaining charge spread among several adjacent pixels. We have developed [4] an algorithm to recover full energy resolution in case 1 by requiring for the detection of an event that all charge is within a single pixel and that the sum of the eight adjacent pixels be consistent with zero signal. This reduces the quantum efficiency somewhat [6]. For the same data, we recover the maximum quantum efficiency by adding charge from all contiguous pixels which are above background. In case 2, this gives us a \sqrt{N} ($N = 4$ to 9) degradation in energy resolution due to the additional noise from the multiple read-out; and in case 3, this gives a "plateau" or "tail" in the energy response below the true energy of the incident photon.

The ideal solution to the above losses of quantum efficiency and energy resolution would be to use a thick (100 to 250 μm), back-side illuminated chip which is fully depleted so that all charge liberated by an X-ray interaction would be driven by internal electric fields up to the buried channel region near the front electrodes. The backside must have only a thin, fairly uniform dead layer. We found that the Westinghouse, Advanced Technology Laboratory, was already studying such a chip under contracts to NIH and Los Alamos. We therefore gave them a

contract to manufacture such CCDs for us to evaluate.

If we anticipate that AXAF will carry a wide field imaging proportional counter with 10 arcsec resolution, there will be a need to cover the central 20 x 20 arcmin (60 x 60 mm) with a high resolution imager, since the telescope resolution is better than 10 arcsec in this region. The linear field which a single CCD chip might cover is limited to the range of 1 to 4 arcmin. This limit is fundamentally imposed by the manufacturing yield of large, two-dimensional arrays. However, anticipating requirements to read the entire chip in times of order 0.1 second at frequencies ≤ 1 MHz, implies desirable chip sizes of no more than 10^6 pixels ($< 2.5 \times 2.5$ arcmin). Our concept would be to configure a "checkerboard" array of chips to whatever size is reasonable within telemetry, cooling, power, and cost constraints. Two offset exposures can be made if it is desired to obtain complete sky coverage. We anticipate that a CCD will have absolute photometric stability to much greater than the precision required to analyze such an observation.

1.3 Summary and Conclusions

In this project we have accomplished the following: 1) surveyed existing CCDs and identified the three most likely to serve as X-ray imagers; 2) constructed an electronic camera control and computer interface, including software to drive a Fairchild 211 CCD; 3) constructed a vacuum mounting and cooling

system which will accommodate different chips; 4) obtained quantitative data on the performance of the cooling and electronics systems and performed necessary rework; 5) obtained X-ray performance data on the Fairchild 211 chip; 6) let a subcontract to Westinghouse to make a fully depleted CCD area imager and monitored their progress, including their successful fabrication of a deeply-depleted linear CCD; 7) adapted our camera system as necessary to accommodate the Westinghouse chips and developed NOVA software to operate the camera and display and analyze the imaging data.

Our general conclusions are that CCDs indeed offer the potential as single photon, X-ray imagers for X-ray astronomy telescopes. We have demonstrated single photon detection, X-ray imaging, high quantum efficiency, and that the energy resolution is at least comparable to a gas proportional counter, all in the 3 to 6 keV range. However, the problems of complete charge collection and transfer are quite significant and require further investigation before CCDs can demonstrate energy resolution comparable to a conventional Si(Li) solid state detector. The Westinghouse chips we obtained displayed an enhanced depletion depth, but were not in fact fully depleted. Some specific design and process errors have been identified; however, additional problems with noise and charge transfer have prevented a total characterization of these chips.

Industry is continuing to advance the CCD state of the art. In particular, other companies are now attempting to produce deep-depleted chips. In our continuing investigations we will reconsider all available chips as candidates for space-borne imagers.

We have found that the electronics (i.e., timing, analog processing, and microprocessor controller with its software) requires system considerations specific to an individual chip. We therefore feel that significant research remains before the feasibility of a large (e.g., 100 chips) mosaic can be demonstrated.

The remainder of this report consists of the specific accomplishments of this project. These have been previously reported in our two semi-annual progress reports. Because of the success of this project, the High Energy Astrophysics Division is now considering CCDs along with other high-resolution imaging detectors as candidates for X-ray astronomy missions. Continuing research on CCD imagers is now being performed under NASA contract NASW-3000, "Continued Development of Advanced, High Resolution Detectors for X-ray Astronomy", with Drs. S.S. Murray and D.A. Schwartz as Co-Principal Investigators.

2.0 SPECIFIC ACCOMPLISHMENTS

2.1 Study of Available Chips

We identified three chips with which to carry out laboratory X-ray evaluations. The Westinghouse fully-depleted area imager will be discussed in section 2.6. The two other chips, an RCA 512 x 320 array and the Fairchild 211 190 x 244 array, were chosen because of their large format and "off the shelf" availability. For actual flight use, the larger Fairchild 221 array would be selected over the 211. The 221 device has 380 x 488 pixels and could be used in a "filled array" mode, without the dead space of the interline transfer registers. We expected the RCA and Fairchild devices to be comparable to the ITEK/Bell Northern Research (BNR) 719 CCD which we had previously tested [4,6]. Front-illumination of these devices limits their useful range to 0.9 to 8 keV, and they have the quantum efficiency and energy resolution limitations mentioned in section 1.2. Nevertheless, they are qualitatively superior to previous high resolution imagers for this energy range. The format of the ITEK/BNR chip is much too small for useful application; however, ITEK has developed one means of mosaicing many chips for their surveillance applications. Also, BNR is now studying the development of a totally depleted chip because of the consequent improvement in infrared response. We have maintained conversations with ITEK to track these developments, and to plan eventual X-ray testing of any successful chips.

We were unable to obtain any thinned, back-side illuminated CCDs for evaluation. Communications with both Texas Instruments and JPL, over the last several years, reveals that none of their 400 x 400, 500 x 500, or 800 x 800 arrays would ever be available for our applications. RCA had recently announced the availability of thinned devices for optical application; however, their back-side illuminated device was mounted on glass for mechanical integrity and therefore would not respond to X-rays. Back-side illumination is necessary to extend the X-ray sensitivity down to about 200 eV. A thinned ($10\ \mu\text{m}$) device will have a high quantum efficiency up to about 4 keV, but will have significantly reduced sensitivity to iron K-lines at redshifts less than a few tenths. Therefore, we planned to defer testing of a thinned device until after we studied a totally depleted, back-side illuminated CCD.

Other companies which we contacted at the initiation of this project were Hughes Aircraft, Reticon, Rockwell, and General Electric. The first two companies were developing arrays under special contracts. It remained to be seen if those developments would be successful, and if the devices would then be available at reasonable cost for X-ray applications. A group at Princeton had done some testing of a 110 x 110 Rockwell array, and found a problem, possibly fundamental, with the loss of charge transfer efficiency when the device was cooled. We had observed a similar effect with the one ITEK/BNR 719 chip which we tested.

General Electric makes a "Charge Injection Device" (CID) whose main distinguishing features are random access to pixels and non-destructive readout. However, the architecture which allows this necessitates a large lumped capacitance and therefore high noise per individual readout. Since the device is not self-triggered, we cannot use the random access to save scanning the entire two-dimensional array. This device would be worth testing if and only if the single readout noise could be as low (< 50 electrons rms) as a CCD. It is possible, in principle, that multiple non-destructive readouts of individual pixels could be used to achieve the noise reduction; however, this would complicate and slow down the electronics.

The state of the art has continued to advance during the course of the present investigation. In our future work we will continue to look at what CCDs are readily available. In particular, Hughes and Rockwell have both progressed to the point where they should be reconsidered for X-ray applications.

To economize our efforts we performed some testing of the RCA SID 51232 using the camera system developed by the Optical Infrared Division of the Smithsonian Astrophysical Observatory for their applications as an optical image detector. For X-ray application, we noticed that the events were smeared over a number of pixels, and that the smearing increased for pixels that required more transfers before reaching the on-chip preamp. We

believe this is caused by trapping states. It was found that about 1000 electrons "thin zero" is needed to fill these trapping states, with a concomittant additional shot noise term of 30 electrons rms. Although "fat zero" of about 20% of full well is known to be necessary for surface channel CCDs, we desire that the thin zero signal itself be negligible compared to the noise terms.

Again, developments by RCA in the last two years, e.g., of thinned, backside illuminated chips, requires that they be carefully reconsidered for our future work.

2.2 CCD Camera

We constructed a complete electronic system, which allowed manual test operation of the Fairchild CCD 211 190 x 244 chip in a hardwired mode. However, the system incorporated a microprocessor, and was designed so that it could become increasingly general and automatic as we implemented interfaces from the microprocessor to the other elements, along with appropriate software development. It should be particularly easy to upgrade the system to operate the larger Fairchild 221 chip.

Figure 3 is a photograph of the CCD camera system, prior to installation of the microprocessor. Camera control amounts to setting the exposure time (any multiple of 40 milliseconds, including zero), number of frames to be taken (1 to 99, or

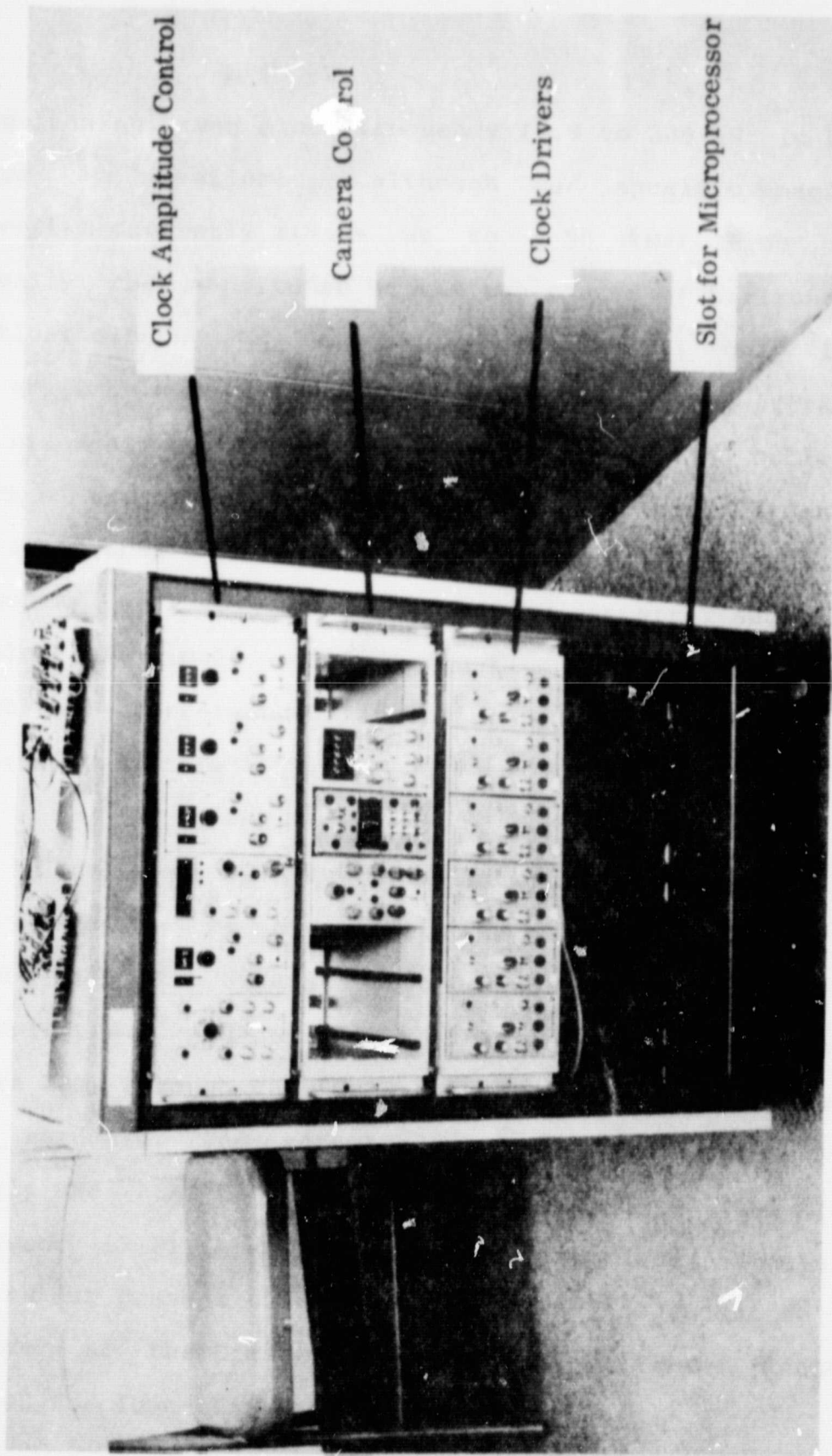


Figure 3. CCD camera system hardwired for the Fairchild 211 CCD.

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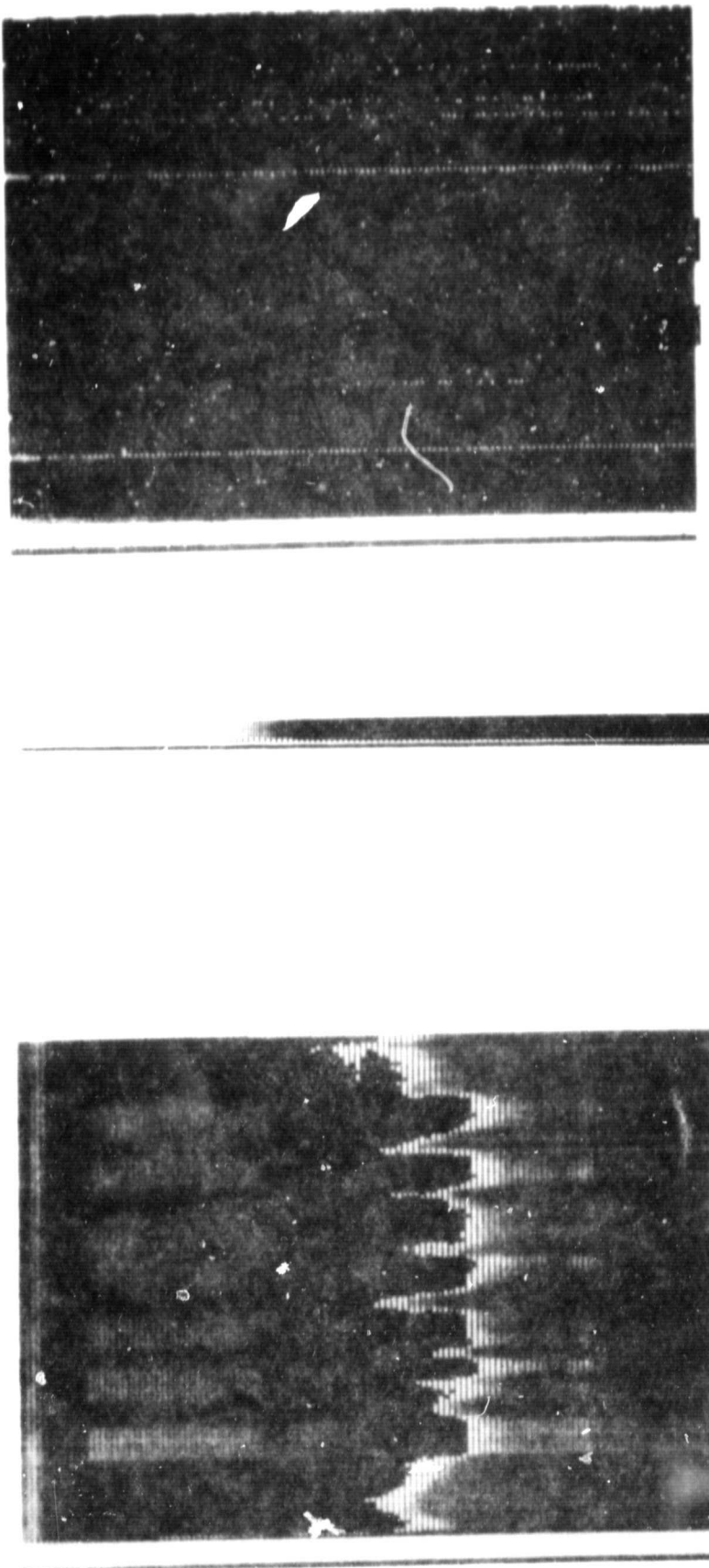
free-running), and clock frequency (0.8 to 205 kHz in factor of 2 steps is available, although our specific microprocessor algorithm currently limits us to ≤ 50 kHz). We can adjust manually the amplitudes of the two phases of horizontal clocks, vertical clocks, and photogate clock. The 211 chip is shifted out as if it were a 256 x 256 array. Some of the extra transfers are necessary when going from line to line. The software keeps track of exactly which shifts represent valid pixel measurements, and loads them into a random access memory (RAM). For diagnostic purposes, we have a digital to analog converter and display, and a selectable single pixel trigger. We can therefore verify functional performance, including optical imaging, without an external computer.

We utilize a NOVA computer for our basic data acquisition and analysis. We have constructed a special purpose interface board between the NOVA and microprocessor. We can interrupt the microprocessor, and cause it to transfer a frame of data from the camera RAM, through the NOVA and thence to disk storage. The NOVA hardware, and software, and our 4 gray level display are largely the HEAO-B ground support equipment real-time image processor (RIP). We have expended significant efforts to adapt them to our present usage, including the incorporation of some features of the Einstein data analysis software. Magnetic tape is used for long-term data storage.

Figure 4 was made by taking our magnetic tapes to the Einstein analysis computer and generating a hard copy output of the display. The data were obtained at room temperature, with optical illumination of the chip. Figure 4A shows good optical focus on a target that reads "High Voltage". Because of a large gradient in the optical illumination, the lower half of the picture saturates the selected gray scale. Figure 4B displays the difference of two dark frames. This picture should be "flat", except for system noise. In addition, we can see two prominent and seven other columns where some blooming (vertical streaks) occurs. Saturation, large shot noise, or non-stationary dark current effects prevent two identical exposures from cancelling exactly for these columns. We would expect these to "clean up" with cooling; however, we would not consider 9 "dead" columns out of the 190 to be a significant compromise of the CCD performance.

2.3 CCD Mounting and Cooling

Figure 5 is a photograph of the CCD 211 in its initial vacuum mounting. The CCD chip, its socket, and the chip interface board are easily changeable. The interface board essentially maps the specific CCD pin connections to the fixed electrical feedthroughs. We initially had the first stage off-chip video amplifier on this card. The cooling port was connected to a large dewar of liquid nitrogen. When a valve was opened by a control unit, vapor pressure forced liquid nitrogen



B

A

Figure 4. Fairchild 211, optical illumination at room temperature.
A: Focused on a sign reading "High Voltage". B: Flat field obtained as the difference of two dark frames.

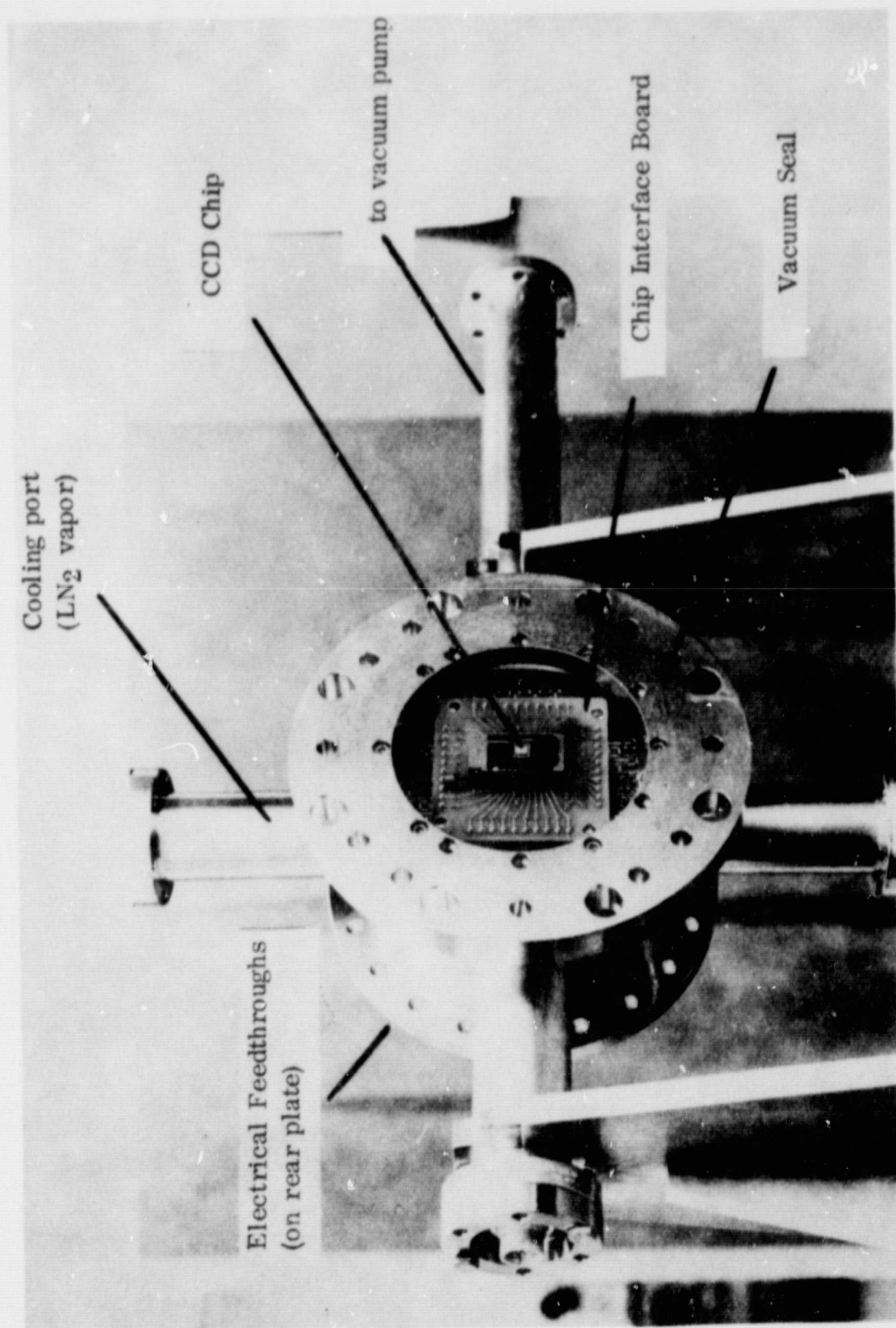


Figure 5. CCD vacuum mount.

vapor through a heat exchanger. The heat exchanger/control unit was a hybrid between a standard Products for Research unit and special parts which we designed and machined because of our envelope and vacuum constraints. We did not achieve stable operation, e.g., liquid nitrogen was observed to go through the heat exchanger and out the exit port (bottom of Figure 5). The diagnosis of this problem required installation of temperature sensors, and subsequent analysis (see section 2.4.1).

The vacuum seal is designed either to mount to the X-ray tubes available in our HEAD labs, or to take a plate with either an optical lens, or a recessed Fe^{55} X-ray source. The system was successfully operated at 5 microns pressure, and the observed decrease in the dark current verified that the chip was being cooled.

2.4 System Analysis and Rework

The previously constructed electronic system and vacuum cooling mount for the Fairchild 211 CCD is collectively referred to as the "camera". It was necessary to acquire some performance data and to rework our original system in the areas of cooling and electronic system noise.

2.4.1 Cooling

Our cooling system was intended to allow a wide range of operation in the laboratory, rather than to simulate a practical

means of space-borne cooling. In the initial system we attempted to copy one previously used for an optical CCD camera which we developed in collaboration with the Optical/Infrared division at SAO. This led to a hybrid consisting of a standard Products for Research liquid nitrogen vapor heat exchanger and controller, plus vacuum and insulator parts which we custom built. It was noticed that this system was very unstable. Our first step in remedying this problem was to instrument the cold finger, CCD ceramic, and off-chip amplifier (which was mounted within the vacuum) with temperature sensors. We found that the off-chip amplifier was overheating, which was corrected by providing a suitable heat sink. The cold finger was found to cycle with an amplitude of 20° to 120° C on time scales of 40 to 90 minutes. We determined that the basic problem was that the Products for Research unit is not designed for vacuum use. In its usual optical instrumentation configuration, convection causes very short cycle times for delivering the liquid nitrogen vapor, leading to $\pm 1^{\circ}$ C temperature stability. In our application, after initial delivery the heat exchanger stayed cold for so long that the flow pipe, and the liquid nitrogen vapor inside it, became warmer than the heat exchanger and therefore the command to cool initially caused warmer vapor to be delivered. Eventually the vapor is delivered near liquid nitrogen temperature but at that time the exchanger is quite warm and the controller delivers so much vapor that the system overshoots the set point.

As a result, it was necessary to redesign the cooling system. We now mount the CCD so that the backside ceramic is in good thermal contact with a short cold finger which is bolted to a large mass containing liquid nitrogen. The heat exchanger is mounted to the outside vacuum chamber by means of thin stainless steel tubing and bellows, and the heat gain is such that usage of liquid nitrogen is of the order of 1 to 2 liters per hour with the detector near -190° C. A heater wrapped around the detector cold finger provides local heating which allows stable operation at a controllable temperature between -190° C and about -150° C. Operation at higher temperatures is effected by inserting a thermal insulator between the cold finger and heat exchanger. Temperature stability is better than 0.1° C over timescales of about 1 hour, once the thermal equilibrium point has been reached (< 1 hour from chamber pump-down). Consumption of liquid nitrogen is about 3 liters per hour for operation at -110° C.

2.4.2 System Noise

We have found that consideration of "system noise" for a CCD camera logically divides into three parts: electronic noise injected by the off-chip system, and which may be present even without an operating chip; noise injected in the CCD itself, over which we have no control; and noise arising anywhere in the system due to improper or non-optimum operation of any given chip. The last two noise areas depend critically on the specific type of chip (and to some extent on each individual chip) and

therefore must be discussed in connection with each CCD. However, our first step was to reduce electronic noise injected by our system.

Figure 6 shows the analog processing chain. Our goal is for a system noise less than 25 electrons equivalent rms (or an equivalent energy resolution of 210 eV FWHM). Since a typical CCD on-chip amplifier conversion gain is equivalent to about $1\mu\text{V}$ per electron, our noise goal is $25\mu\text{V}$ rms equivalent at the off-chip preamp input, or 8 mV rms equivalent at the input to the analog to digital converter, after a nominal system gain of 320. Not shown in Figure 6 are the logic signals, driven by the microprocessor, which control the sample-and-hold and analog to digital conversion operations.

Initial tests of system noise, when operated without a CCD, led to implementation of the following improvements:

- 1) Replacement of a sample-and-hold module located just before the analog to digital converter. The original module appeared to produce a time-varying signal amplitude which implied unreliable operations and a deceptive noise level.
- 2) A change to the sample-and-hold operation such that continuous sampling is effected, thus eliminating droop during the time gap between successive frames. This droop was responsible for the fact that the first of any series of frames had a time-varying DC level.

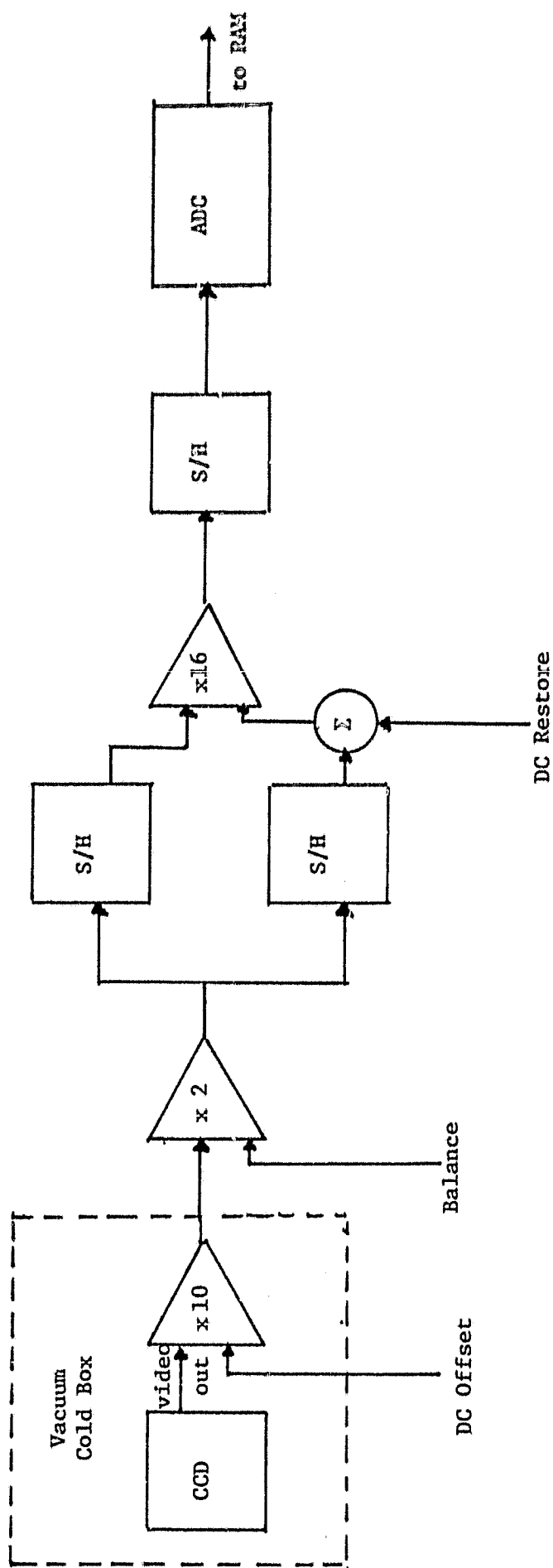


Figure 6. CCD analog processing: correlated double sampling, with delta-function sample.

- 3) Additional shielding of the video-in line from the off-chip preamp to the main processing module.
- 4) Addition of a low-pass filter at the video input of the processing module.
- 5) A new interface card for the Fairchild CCD. This card has the same circuit design as the old card, except for the new op-amp with better driving capability and low noise Vishay resistors. Circuit connection is by printed circuits instead of bus wires and the pin configuration was modified for better signal isolation.
- 6) New ± 15 V power supply for the off-chip preamp.
- 7) Repositioning of some cables from the detector vacuum chamber to the processing module to reduce pick-up.
- 8) Shorter cables between the analog processing module, the voltage supplies, and the detector vacuum chamber, together with additional shielding.
- 9) A clean up of system wiring and grounding errors.

With no chip connected, we measure an rms noise of roughly $200 \mu\text{V}$, after the $\times 10$ off-chip preamp.

We initially set up the correlated double sample to use delta-function samples of the signal and reset voltages. However, the best signal to noise arises by integrating or averaging each sample [7,8], so we added a gated integrator, as an option, to perform the samples. We did not perform testing

using the gated integrator during this program.

2.5 Performance of the Fairchild 211

2.5.1 Functional

In order to acquire quantitative information about a CCD as an X-ray imager, and to test our single photon camera system, we performed our initial measurements on a commercially available device, the Fairchild CCD 211. This is a 190 x 244 area array, with an interline transfer readout. We reported these results at the SPIE Annual Technical Symposium in San Diego [9]. We expected that the floating gate amplifier (FGA) would give a very low system noise [10]. However, the 211 chip which we obtained was from the late 1979 production lot, and had an architecture modified to be more nearly that of the CCD 221, a 380 x 488 array. This necessitated some rework of our interface, or "personality card", to accommodate changes in pin connections and operation. Problems were experienced with these chips with regard to stability of their on-chip floating gate amplifier, and the reproducibility of the results we obtained may be questionable. In particular, we measured a charge conversion gain of the floating gate amplifier of $1.3 \mu\text{V}$ per electron. We note that this sensitivity is comparable to the nominal value for the "old" CCD 211, whereas the "new" CCD 211 should have a sensitivity which is higher by a factor of about 4. If all other noise sources remained at a fixed level (in μV rms), we would

expect the noise equivalent electrons to be reduced for a chip which showed nominal performance.

For the particular Fairchild 211 chip we tested, the characteristics of the FGA changed on the time scale of weeks to days. It was necessary to readjust bias and clock voltages to make the chip operate. We observed a general degradation of performance, and the chip finally became non-functional after several months. We do not expect this degradation to be a normal feature of a CCD [10]. Discussions with Fairchild confirm this point of view in as much as this lot of CCD was defective and not representative.

Correct setting, by empirical means, of the horizontal (ϕ_H) and vertical (ϕ_V) clock levels is a key to CCD operation. The clock driver levels were originally set to those recommended in the CCD 211 data sheet, and later to those recommended for the CCD 221. Neither of these sets of voltages produced optical images from the chip. However, optical imaging was successful for ϕ_{H_1} and ϕ_{H_2} settings around 6V and for ϕ_{V_1} and ϕ_{V_2} settings at about 7V. The photogate upper level (ϕ_{PG}) was set to 5V, and that of the bias electrode (ϕ_{BE}) was set to reduce the level of clock feedthrough at the output. All lower clock levels were set near 0V.

Initial X-ray testing was performed by placing radioactive

sources (Fe^{55} for 5.9 keV and Cd^{109} for 22 keV) in front of the thin beryllium or mylar windows on the CCD vacuum chamber. The clock levels were adjusted to compensate for the following problems:

- 1) Erratic DC level changes in CCD output caused by the presence of X-rays (a possible manifestation of instability in the FGA).
- 2) An overshoot/undershoot in the single-pixel X-ray response (a lesser manifestation of 1).
- 3) A steady drift in DC level during the frame readout.
- 4) A change in DC level between dark frames and those exposed to X-rays.

Problems 1 and 2 were corrected by adjustment of ϕ_{H_2} , with simultaneous changes of ϕ_{BE} to reduce clock feedthrough, and to maintain the same floating gate amplifier gain. Following adjustments to ϕ_{H_2} , ϕ_{BE} , and V_{SF} , adjustment was usually necessary to ϕ_{V_1} and ϕ_{V_2} , in order to give a constant baseline during readout of each vertical line. The clock voltage ϕ_{H_1} and ϕ_{PG} were generally held constant, as was the bias voltage V_{DD} .

Problem 3 was addressed by lowering the anti-blooming bias V_{AB} until the DC baseline of the frame output was constant. Adjustment to ϕ_{V_1} and ϕ_{V_2} were often necessary following adjustment to V_{AB} . We note that the baseline change introduced in the presence of X-rays may be similar to the phenomenon of permanent baseline change previously noted by Koppel [11] and in the RCA

SID51232, and attributed to photogenerated charge trapped in the dielectric SiO layers. In the present case, however, the baseline change is not permanent and returns to its previous level when X-radiation is no longer present, implying that the trapped charge can be cleared by sweeping the pixels and vertical shift registers. This temporary shift in baseline, of order a few mV at the CCD output, occurs for integration times of a few seconds to minutes under X-ray fluxes of about 10^4 photons/cm²/sec (and is a shift in both the "signal" and "reset" levels). A permanent baseline shift may also have been present, but was not looked for or noticed during a total exposure of about 10^8 photons/cm².

2.5.2 X-ray Results

The digitized pixel amplitudes of each frame of data were used to plot histograms of the number of pixels versus the pulse height in a single pixel. Examples are shown in Figure 7, which plots the single-pixel response to X-rays of energies 3 keV and 6 keV. The integration times for these frames of data were generally of the order of a few seconds to a few tens of seconds. At temperatures below -100° C, where we operate, there is zero dark current accumulation for these integration times. The FWHM of the X-ray peak for the 3 and 6 keV events is, to within the accuracy of the measurement, the same as that of the system noise peak, about 1 keV. With a conversion factor of 3.7 eV per electron-hole pair [12], this implies a raw system noise level of

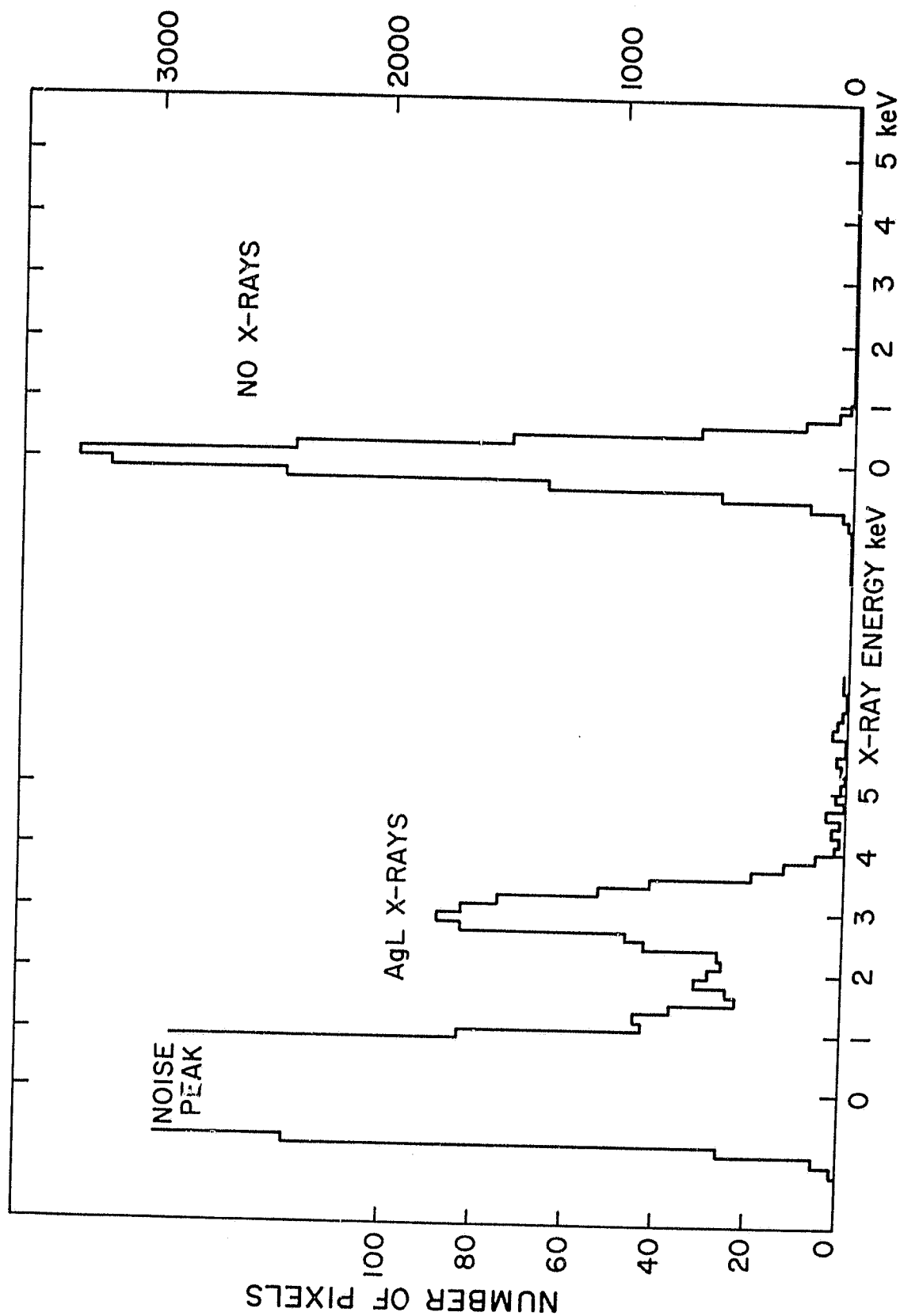


Figure 7a. Response of Fairchild 211 to 3 keV X-ray photons.

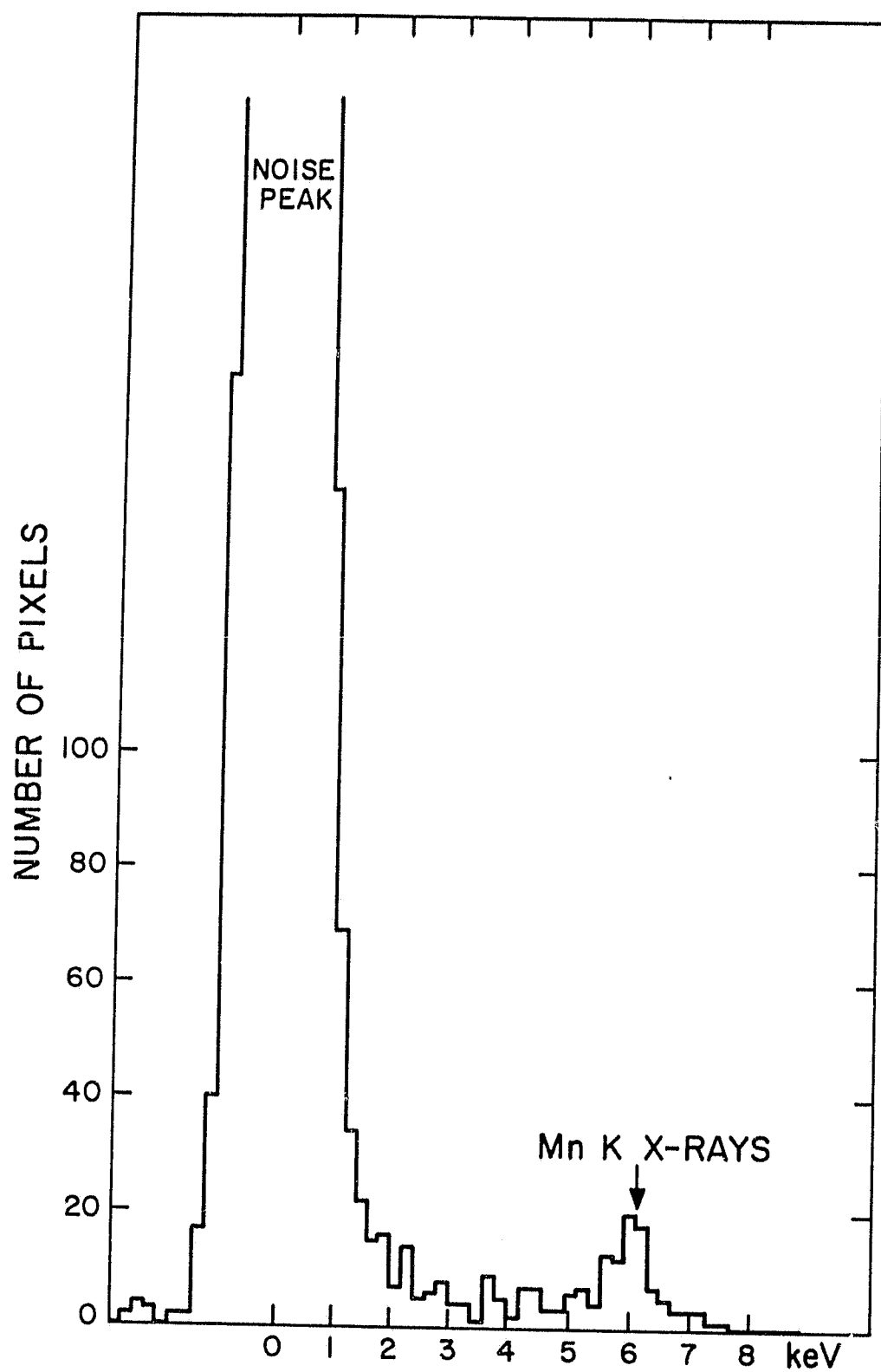


Figure 7b. Response of Fairchild 211 to 6 keV X-ray photons.

about 120 electrons rms. We next correct for baseline changes by computer processing of data. A digital "baseline restoration" can be effected on a line-by-line basis, resulting in a net rms noise level of about 100 electrons per pixel.

The absolute quantum efficiency of X-ray detection by the CCD was measured by monitoring the X-ray flux with a proportional counter. The single-pixel efficiency for 3 keV X-rays was found to be very high, about 80%. This efficiency has been calculated taking the nominal pixel area from the Fairchild data sheet. The corresponding efficiency for single pixel X-ray events at 6 keV was lower, ~30%, which is considerably less than the expected value, considering only the probability for an X-ray to interact in the silicon. The difference between the observed and expected efficiency at 6 keV is due to the spreading of charge over many pixels [4,13,14]. (It was our recognition of this problem [4] that motivated our efforts to obtain totally depleted CCDs.) X-rays of energy greater than about 4 keV will undergo photoelectric interaction mainly beneath the depletion layer, in the silicon substrate. At 6 keV, the X-rays undergo 1/e absorption in 30 microns of silicon. For the resulting cloud of 1700 electrons to be collected in a single pixel, it has to reach the depletion layer before diffusion results in a cloud size greater than a fraction of a pixel in diameter. Solid angle fractioning and recombination losses dominate for larger diffusive cloud diameters. A charge cloud originating in the

silicon bulk will be attenuated due to recombination by a factor $e^{-d/D}$ if it has to travel a distance d to the depletion layer, where D is the electron diffusion length. Estimates of D are in the range 50-100 microns [11,13], much larger than a pixel dimension. Our image displays show that events do occur where charge is shared by at least 2 pixels, proving that some collection takes place from below the depletion layer.

We also verified that the X-ray single pixel amplitude vs energy obeys a linear relation from 6 and 22 keV, through the region of 3 keV. These sets of measurements were made under slightly different clock voltage settings, since the Henke X-ray source was used for the low energy measurements, while radioactive sources were used at 6 and 22 keV during a different run.

One of our key results was the demonstration of the X-ray imaging capability of the CCD. Figure 8 was obtained by placing a metal mask in front of the CCD and illuminating with 3 keV X-rays from the Henke tube source. This picture was built up on the storage scope monitor screen by successive integrations of 4 seconds each (the same data can also be accumulated in a single frame having the same total integration time). The mask was originally used to test the microchannel plate arrays for the Einstein X-ray Observatory (HEAO-B): the HEAO-B acronym is visible near the center of the image. The letters are 25 microns

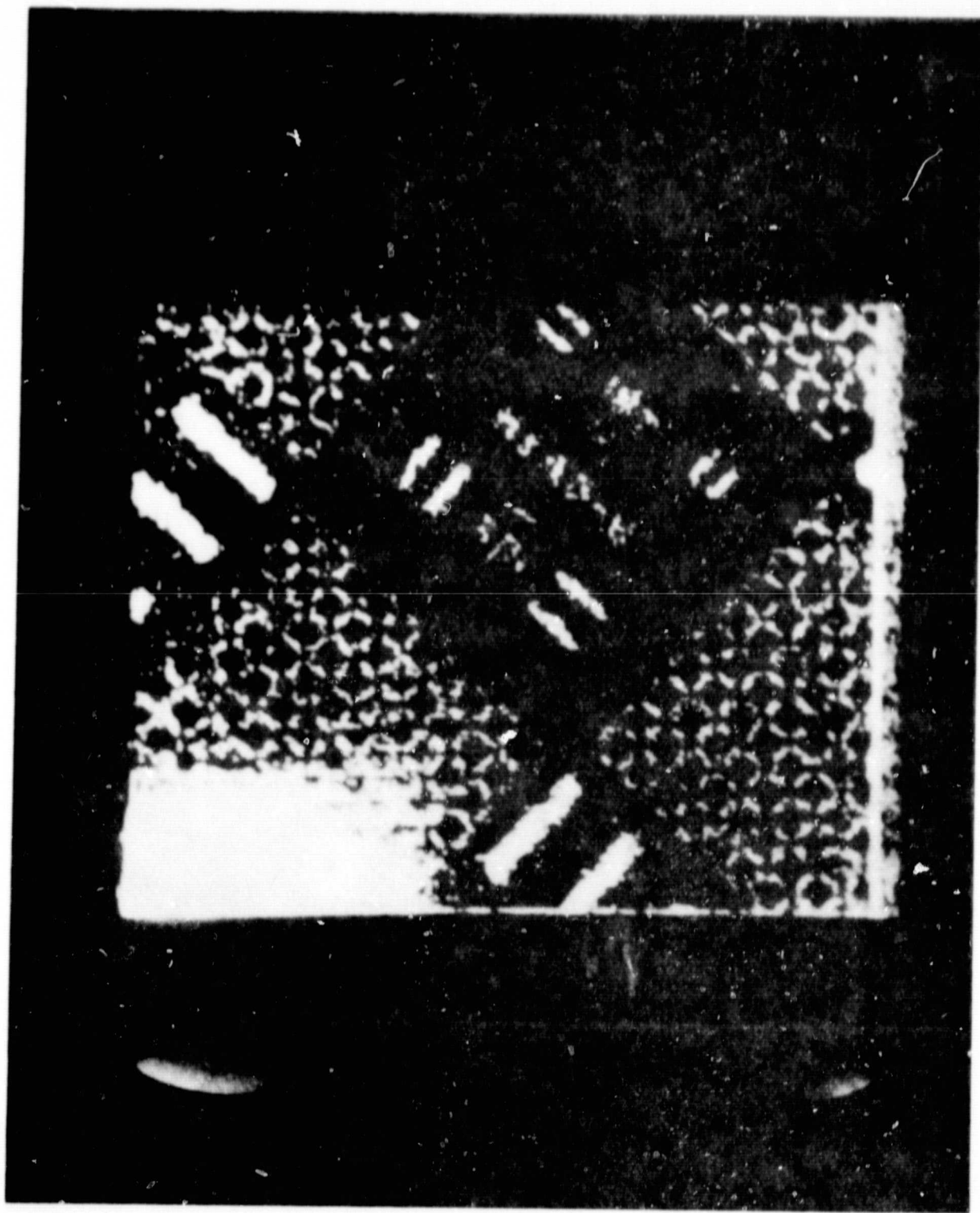


Figure 8. Image in 6 keV X-rays, using the Fairchild 211 CCD.

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wide, comparable to the pixel size of the device under test 14 x 18 microns). The lines beneath the H and B are 75 microns wide, corresponding to about 4 pixels. Since there is no degradation of the image at the furthest point from the FGA, it is concluded that the transfer efficiency is as high for 3 keV X-rays as it is for optical images, i.e., greater than 0.9999. (Note that the bright area at the lower left corner is caused by a small maladjustment of clock amplitudes, and did not appear on other images.)

This high transfer efficiency is of great significance because of the difference in operation for optical and X-ray applications. The X-ray application involves the "infinite-contrast" case where there may be zero charge in all pixels except that in which the X-ray interacts. Therefore, even a low density of traps may strip out charge and "trail" it behind the image, (cf. discussion of RCA chip in section 2.1). In laboratory optical applications there is generally some illumination of every pixel, and therefore charge lost to a trap may be replaced by charge released from a different trap. We have verified that smearing by traps is not important in the Fairchild chip, at our operating readout frequency of 50 kHz.

2.6 Westinghouse Subcontract

As part of our survey to identify existing CCDs as candidates for our X-ray imaging requirements, we contacted

Westinghouse concerning their program to develop a fully-depleted CCD for medical (National Institute of Health) and plasma diagnostic (Los Alamos) applications. The basic principle is to use high purity (less than 10^{12} cm^{-3} background concentration) silicon so that there are no sites of free charge generation available to cancel the electric fields in the bulk silicon. We contracted with them to produce two groups of such chips for our evaluation. Each group (5040 mask set) consisted of several different arrays, 200 and 256 element line arrays, and a 200 x 100 area array. The first group had tin oxide gates, which are optically transparent to allow front- or back-side illumination. The second group had a polysilicon gate structure. The purpose of the latter is to allow standard indium bump bonding techniques to achieve (in the future) a mosaiced array of the 200 x 100 pixel chips.

Westinghouse slipped the delivery schedule of the original contract by about six months. This was due to delays in delivery of high purity silicon to them, and to delays in access to their test facilities. They encountered "learning curve" problems in handling and mounting the chips, and ultimately only two functioning area arrays were delivered to us.

Of overwhelming significance is the fact that Westinghouse successfully made one-dimensional, fully-depleted chips [15]. Figure 9 demonstrates the successful charge transfer in one such

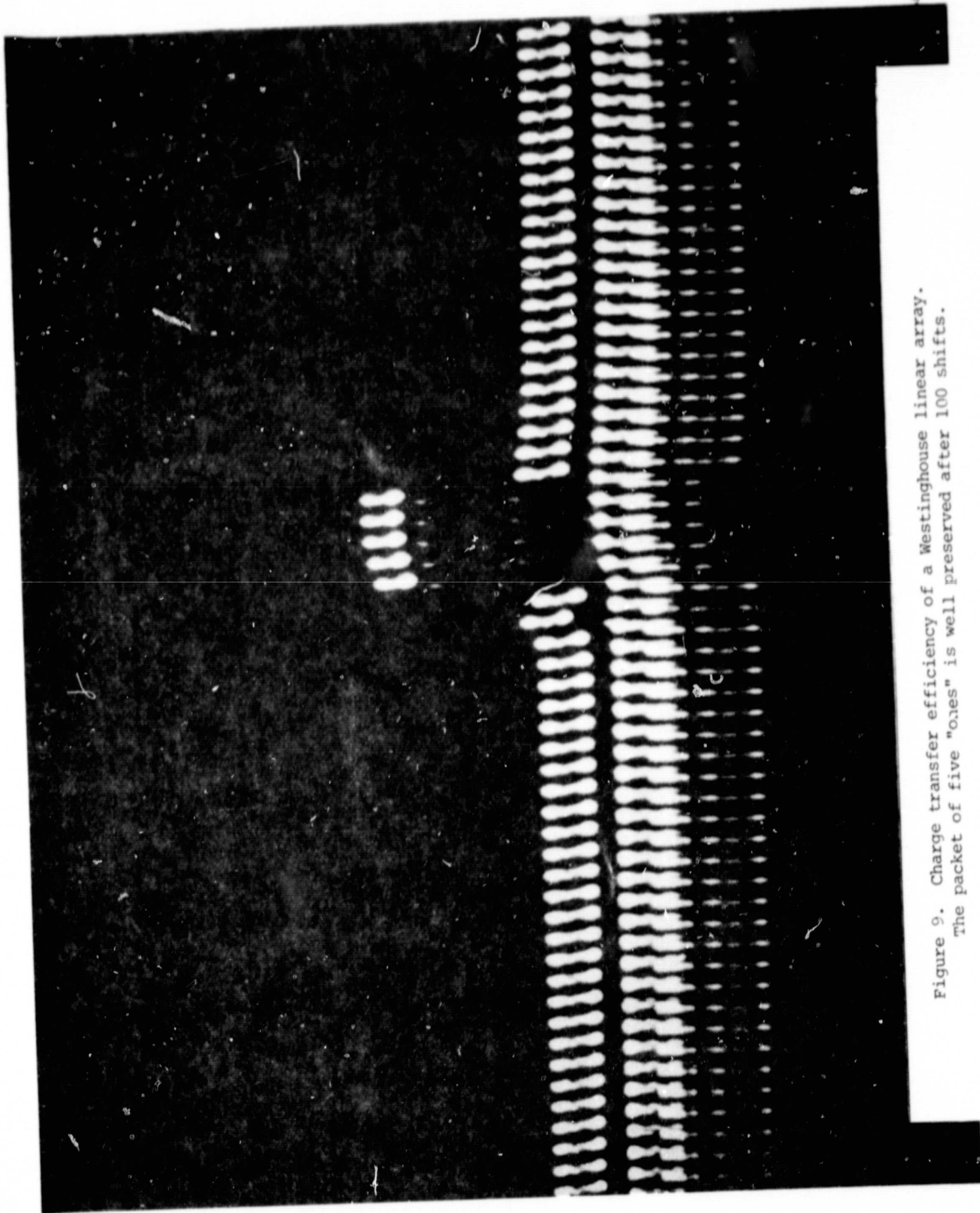


Figure 9. Charge transfer efficiency of a Westinghouse linear array.
The packet of five "ones" is well preserved after 100 shifts.

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chip, at 79° K. They electronically injected charge packets to give 5 ones in a long string of zeros. The top trace shows that these packets are well preserved after shifting through the 100 elements.

The fully depleted chip has a potential drawback in terms of increased dark current. Simply from the standpoint of the increased volume, we might expect 50 times greater dark current. In theory, this could be overcome by cooling an additional $\sim 30^{\circ}$ C if due to bulk impurities. The initial Westinghouse chips have used the (111) crystal lattice, which is known to have high surface state contributions to free charge-carriers, and shows a much higher dark current than expected. Future chips will use the usual (100) lattice, but an acceptably low level of dark current remains to be demonstrated.

Figure 10 demonstrates that the chip is indeed deeply depleted. The top trace shows the output when the chip is back-side illuminated with a narrow slit of white light (with an infrared filter). The response is no more than 5 pixels FWHM, which might be accounted for by finite slit width and reflections in the various optics, since a similar response results when the same chip is front-side illuminated. Since the chip is about 12.5 equivalent pixels thick, without deep depletion the collected charge would diffuse over at least 25 pixels. The mean free path for visible light is less than several microns so that

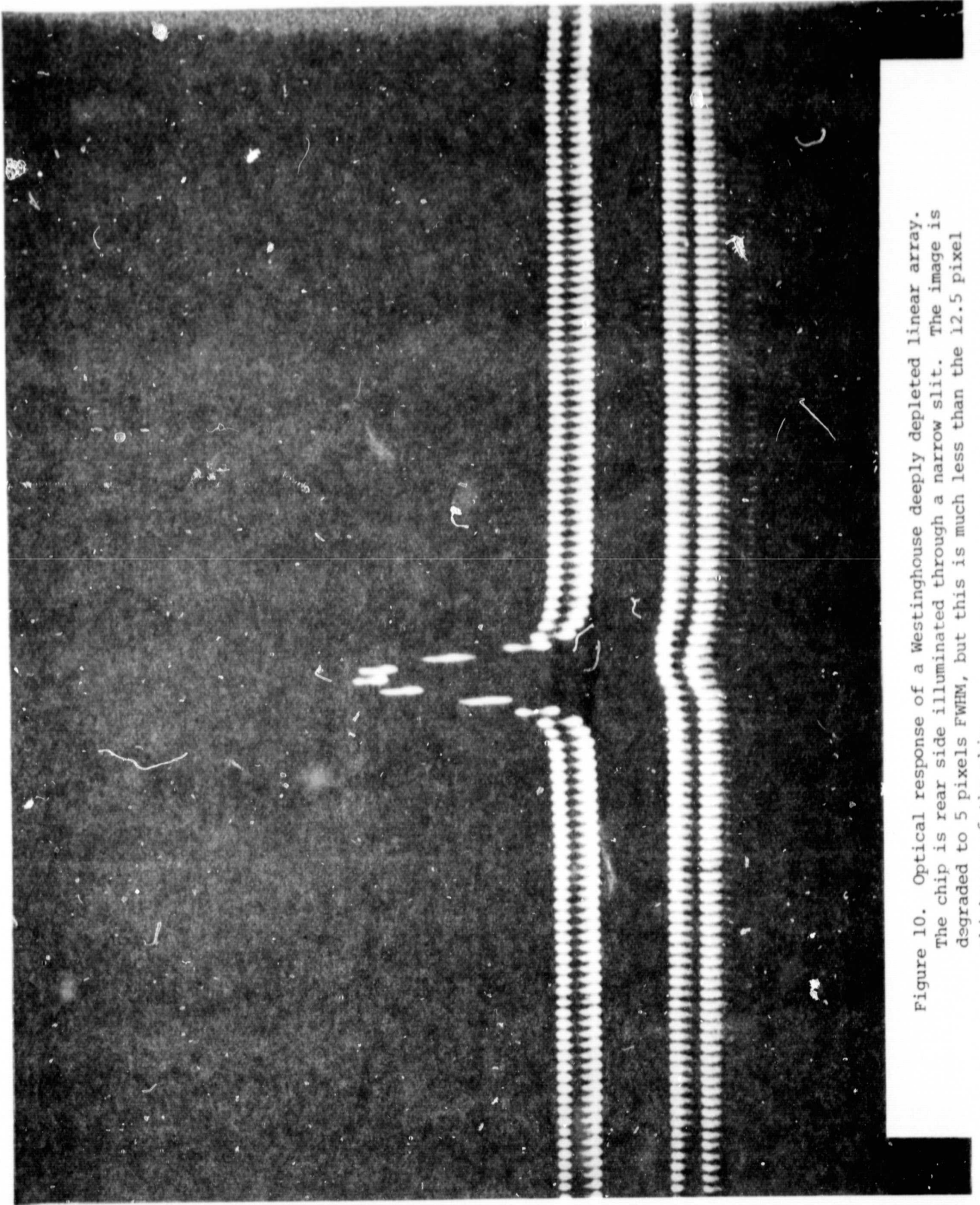


Figure 10. Optical response of a Westinghouse deeply depleted linear array. The chip is rear side illuminated through a narrow slit. The image is degraded to 5 pixels FWHM, but this is much less than the 12.5 pixel thickness of the chip.

released charge must pass through the total thickness of the silicon substrate to reach the photosite. The photogate voltage can actually be de-tuned so that the depletion depth does not extend through the chip, and in this case one does observe the peak to broaden. Westinghouse has reported results from their previous contract [14], and further results on the chips manufactured for us were discussed at the 1980 Los Angeles SPIE meeting [15].

2.7 Camera System for Westinghouse Chips

2.7.1 Microprocessor System

Figure 11 shows a schematic of our microprocessor hardware. The Intel 8086 CPU, input/output board, interrupt controller, EPROM and random access memory storage are purchased as part of the basic system. We designed, laid out, and wired the boards containing the clocks. These are configured under software control, allowing preset counts, phase offsets, and one-shot logic to be implemented. This then provides the appropriate logic signals to standard CCD clock drivers, permitting readout of a variety of different CCDs.

Synchronized with these clocks are the logic signals which control the analog to digital conversion and ultimately read the digitized data into the microprocessor CPU. These logic signals typically have 16 steps of phase control relative to the fastest

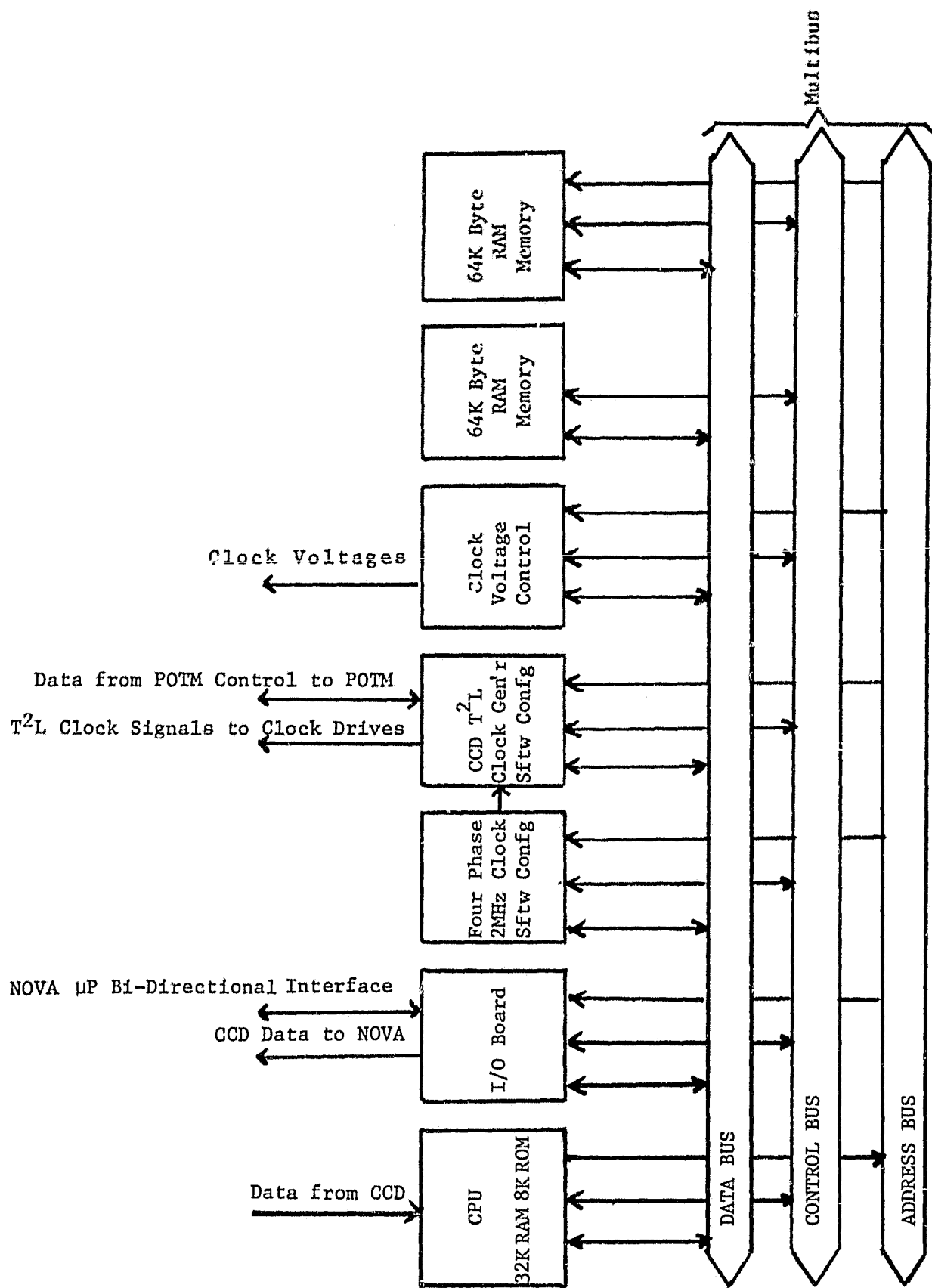


Figure 11. Microprocessor system configuration

shift clock. Our 2 MHz master clock is divided by ten for a maximum readout rate of 200 kHz, with all lower frequencies which can be obtained by dividing by two also available. However, the FIFO buffers and the cycle time of our microprocessor software currently limits us to a maximum rate of 50 kHz. The digitized output of an entire CCD field is stored sequentially in a 64 K byte RAM.

For the Westinghouse 100 x 200 area arrays the microprocessor provides four phase horizontal and vertical clocks which count to 110 x 220, respectively, to allow for some overhead in the shifting to the output register and to the on-chip preamp. Our hardware allows us to take the output from either of the two output chains provided on the chip (but not from both simultaneously). We have not yet implemented software to allow the amplitude of the clock voltages to be driven via the microprocessor.

Figure 12 shows a schematic of the microprocessor software system as set up to drive a chip. Currently the system can respond to a command to load appropriate modules ("subroutines") to operate either the Fairchild 211 or the Westinghouse 100 x 200 arrays. When power is first turned on, or upon reset from the front panel switch, the INITIALIZE routine sets default values for all variable parameters, and starts the chip operating at a high shift frequency to "clean out" the registers. The

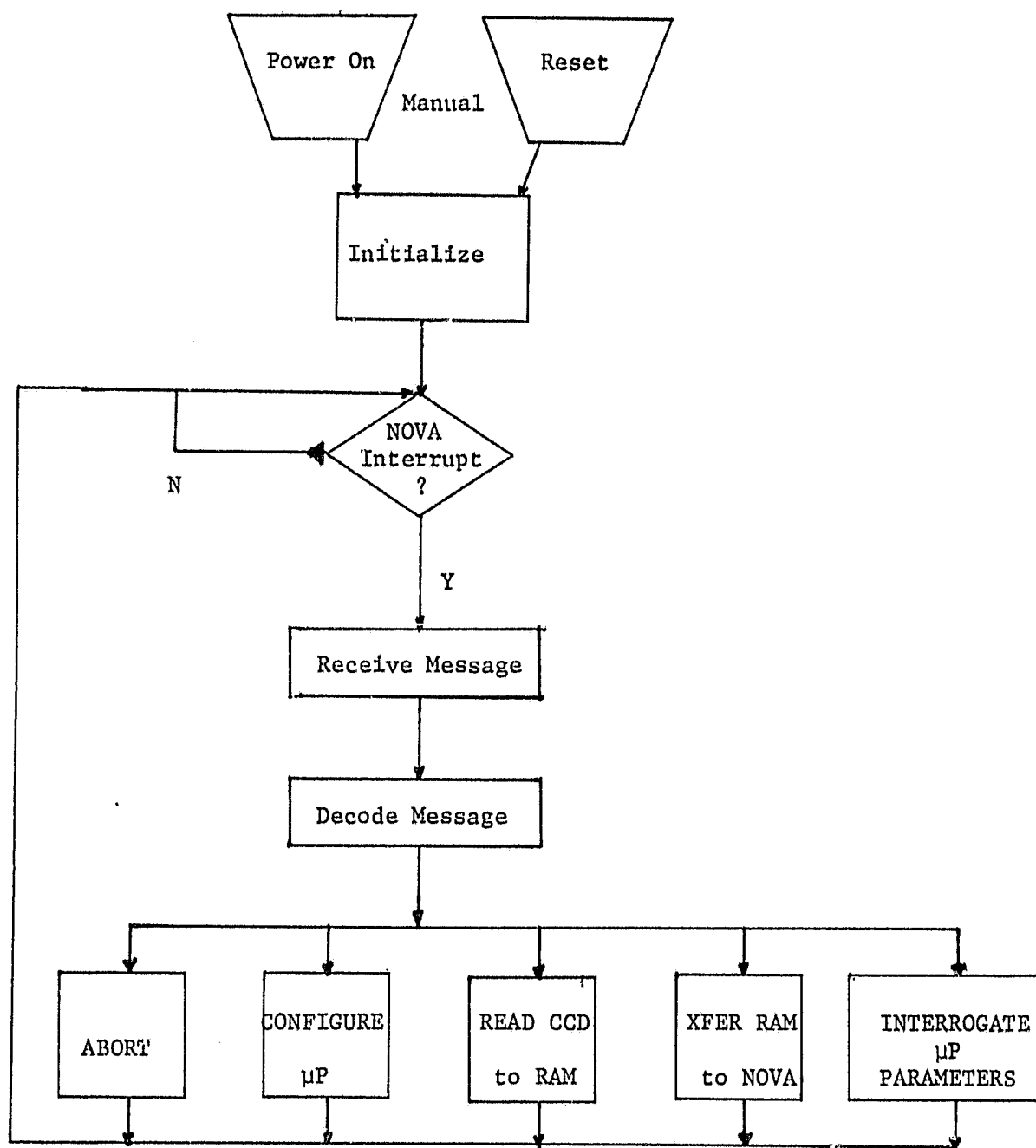


Figure 12. Microprocessor software system

microprocessor then becomes a slave to the NOVA system, waiting for an interrupt. It then accepts a message from the NOVA, decodes it, and calls the appropriate module to execute the command.

Our current CONFIGURE routine allows the following parameters to be specified:

- 1) Integration time, in units of 50 msec, including zero;
- 2) Readout frequency, as $50/2^n$ kHz, $n = 0,1,2,3,4$;
- 3) Number of sweeps to be made to clear the chip prior to starting integration;
- 4) Number of frames to be read into RAM;
- 5) Index of frame to be read out from RAM;
- 6) Identity of chip (Fairchild 211 or Westinghouse);
- 7) Selection of correlated double sampler (delta-function or gated integrator).

The INTERROGATE routine causes the micro to transmit its current value of all these parameters back to the NOVA. When the high order bit of any word (command or parameter) is ON, the ABORT routine is entered and control reverts to the NOVA.

We have developed a Data General standard hardware interface between the NOVA and microprocessor, along with appropriate software protocol. An interface board, resident in the NOVA minicomputer, and a 30 foot cable provide the interconnection

between the NOVA and the microprocessor. This allows the NOVA to send messages to and accept CCD data from the microprocessor. The messages are used to configure and request status of the microprocessor over 16 input/output lines. A second set of 16 input lines permits the NOVA to receive data from the microprocessor via the data channel facility provided in the NOVA. There are two additional sets of four control lines for starting and stopping the message and data move operations. A single signal return line is provided in the cable.

The protocol used to transfer the data considers that every cycle consists of one transfer from the NOVA to the microprocessor and a response transfer from the microprocessor to the NOVA. Each transfer of data to the NOVA generates an interrupt, which can be processed (if there was a request from the microprocessor) or simply cleared without accepting the data. In the idle state the drivers/receivers on both ends are in "receive" state. All messages are initiated from the NOVA end and every message transmitted is echoed back by the microprocessor. Should the microprocessor fail to reply (e.g., power may be off), the NOVA has a software timeout loop which puts the NOVA back into its receive state. This timeout also keeps the program in the NOVA from hanging up in the case where there is no reply due.

2.7.2 Analysis and Control Computer System

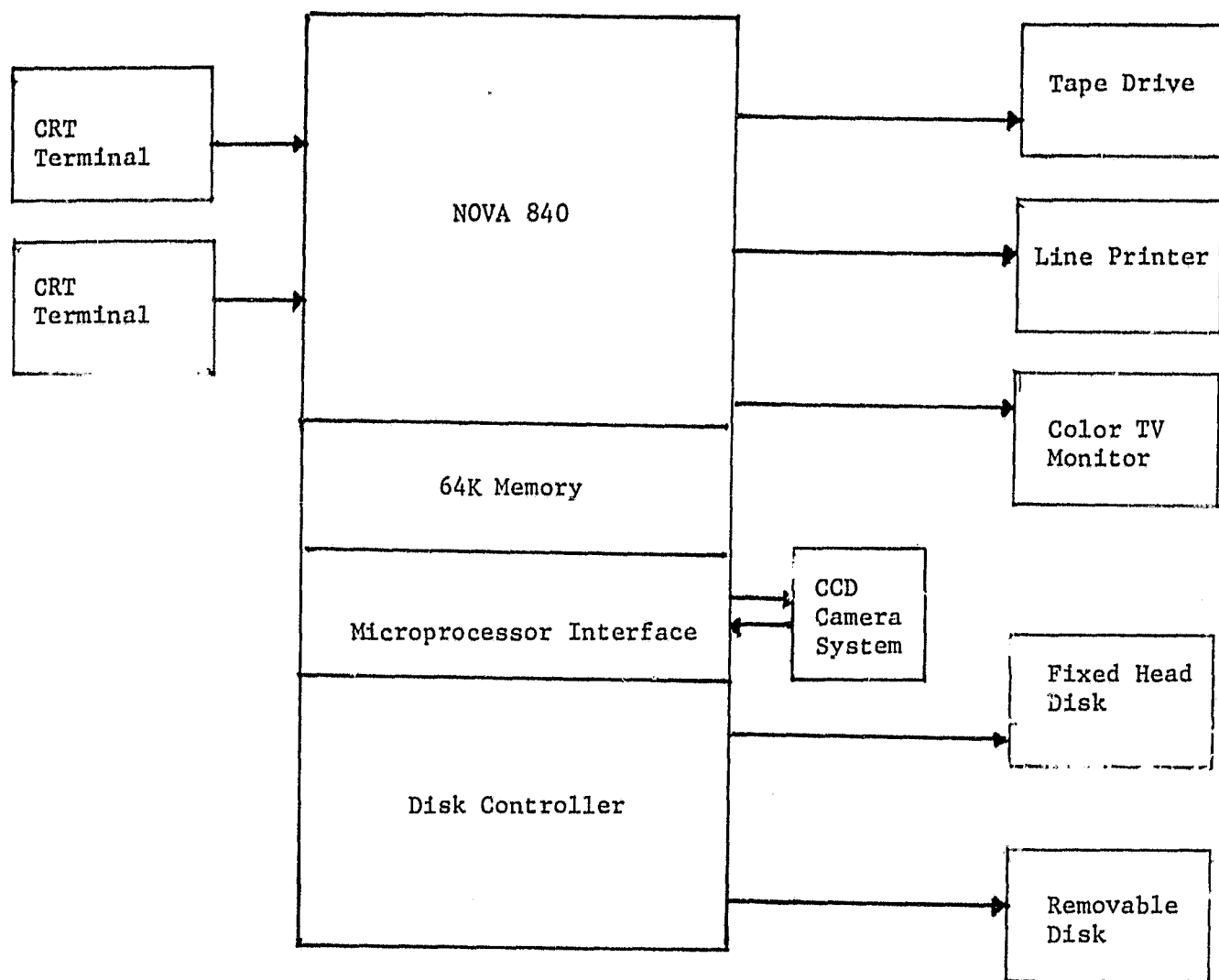


Figure 13. X-ray CCD computer hardware

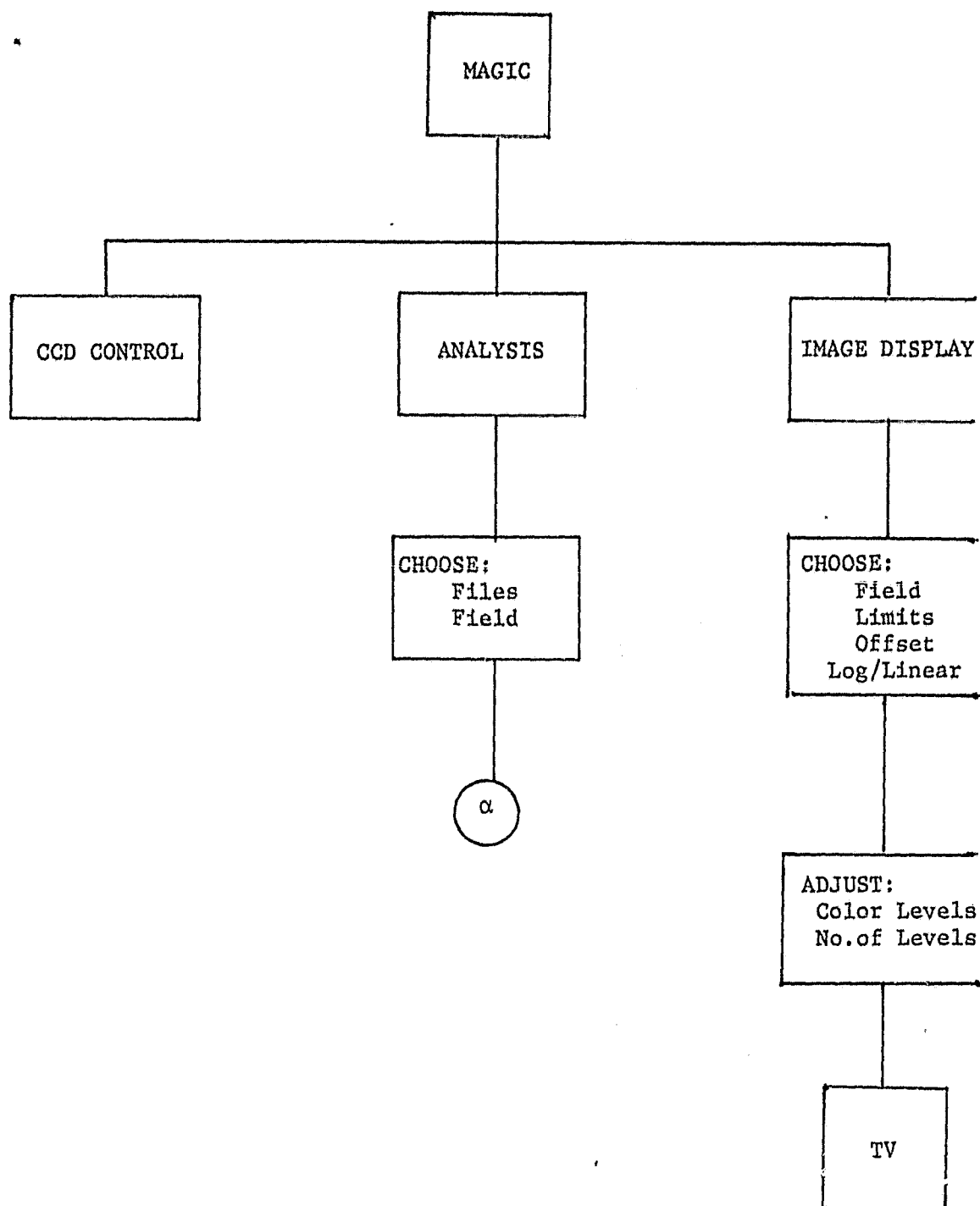


Figure 14. NOVA software functional block diagram

Figure 13 shows a block diagram of our NOVA computer system. The NOVA 840 operating system is mapped RDOS, which allows two users in a foreground/background configuration, each of which has about 30 K words available for application software.

The CCD software system (Figure 14) has been implemented using a new language, MAGIC, developed at SAO to run under the Data General operating system RDOS. It is a general purpose interactive compiler which is an outgrowth of STOIC, itself an extension of FORTH. Like those two languages, it combines the advantages of a completely interactive environment with relatively fast compiled code. Unlike STOIC and FORTH, MAGIC allows the users to write entirely in standard forward notation. The syntax resembles a cross between FORTRAN and PASCAL. MAGIC includes an assembler and all assembly level input/output functions and system calls. MAGIC speeds program development time considerably. Compile time is almost always less than edit time. The user may run part of a program and then interpret or modify any variables and then run another part of the program. New algorithms may be tested at the keyboard before being added to the source. Thus, MAGIC is an ideal language for development and testing of new hardware.

The basic CCD CONTROL program handles all data transfer from the microprocessor to the NOVA, and allows the user to configure the chip by transmitting parameters to the microprocessor. It

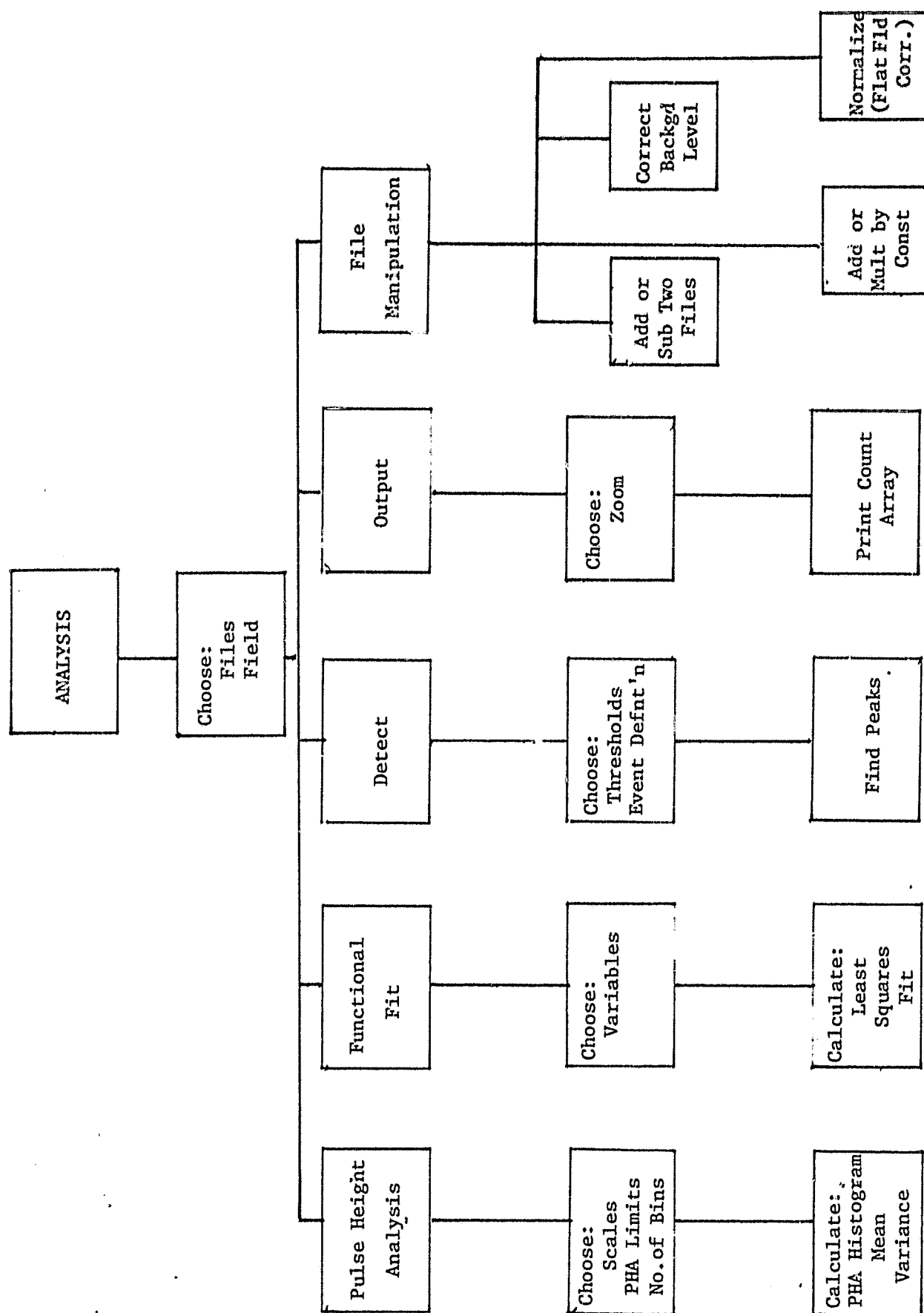


Figure 15. NOVA analysis software functional block diagram

enables the operator at the NOVA terminal to cause the microprocessor to carry out any of the tasks shown in Figure 12.

The CCD analysis and image display systems (Figures 14 and 15) have been developed with general parameters which allow them to handle data from any of a variety of chips, including RCA, Westinghouse, or Fairchild. After setting five basic parameters for the desired chip, all chip-dependent analysis proceeds invisibly to the user. The basic analysis and image display capabilities of the main CCD CONTROL program are supplemented by an additional analysis program and imaging program.

The full analysis capabilities (Figure 15) currently include the following:

- 1) Calculation of means, variances, and standard deviations of pulse heights for (a) any rectangular area of chip, and (b) every line within that area.
- 2) Display of a histogram of pulse heights for any rectangular area of the chip.
- 3) Addition or subtraction of data files to produce a new summed or corrected data file.

The TV imaging capabilities currently consist of sorting into 16 intensity bins using either a linear or log scale and displaying this image on the screen. Any or all of the 16 color levels can be adjusted to highlight features. Also, for

convenience, a calibration bar displaying the color code for each pulse height bin can be displayed with the image. This image may be produced from the data as it is received from the microprocessor or from a data file stored on disk.

2.7.3 Initial Operation

Westinghouse has successfully fabricated a two-dimensional, deeply depleted CCD array [15]. The device was made with the (111) silicon lattice, and with tin oxide gate electrodes. The evidence that the device was fully depleted was demonstrated at Westinghouse by obtaining an "image" of a slit in white light when the 330 μm thick chip was back-side illuminated. The "image" was a video trace on an oscilloscope from different individual lines, and was degraded by about 200 microns, ostensibly due to lack of alignment of the slit axis with vertical columns.

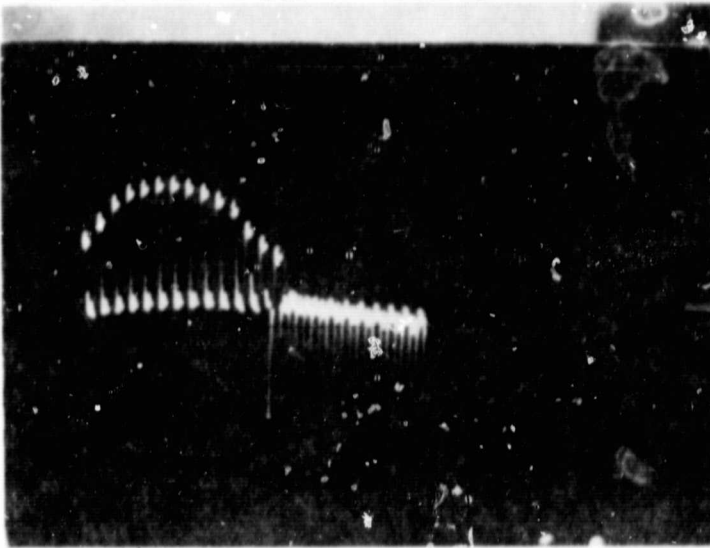
Westinghouse has delivered three of the above chips to SAO. One was non-functional and intended only to check out our cooling system. One other was a functioning, deeply depleted array. The third had severe charge transfer inefficiencies in the horizontal register. We exercised the chip with our camera system in a stand-alone mode (i.e., without the NOVA system) to verify correct logical operation of our camera. After proper adjustment of the horizontal and vertical shifting voltages, we verified that the chip is sensitive to light, when back-side illuminated,

by looking at the chip video output on a scope. Furthermore, Figure 16 shows that the chip images in white light. We placed a pinhole mask of 200 microns diameter over the chip and exercised it with our microprocessor camera system to produce this figure.

The contract with Westinghouse also called for delivery of 100 x 200 CCDs with polysilicon gate structures, and we were told that one lot of chips would be made from the (100) crystal lattice. The polysilicon structure is amenable to present Westinghouse techniques for indium bump bonding to produce focal plane arrays. The significance of the (100) lattice is expected reduction in thermally generated electron-hole pairs from surface states. However, Westinghouse was not able to deliver any of these devices within the resources of the original contract. They have privately told us that they will supply some of these chips for us to test if they become available as an adjunct to their own on-going programs, or in conjunction with follow-up programs funded by us.

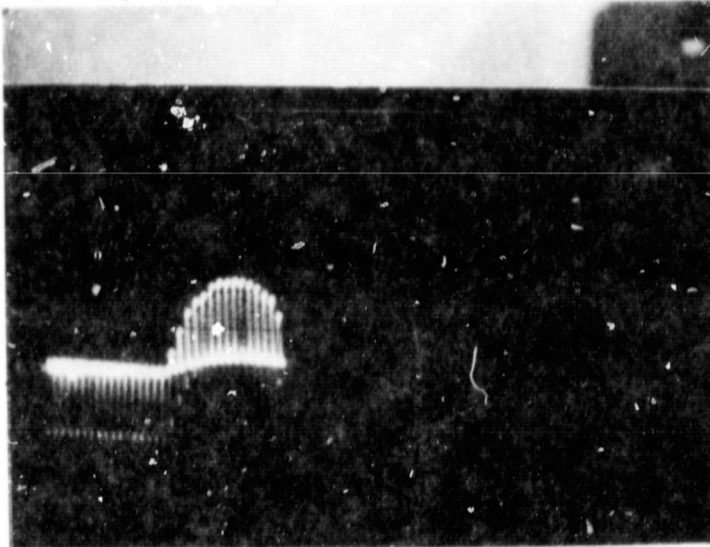
Our X-ray measurements showed that the chips we received were not totally depleted. Cd^{109} and Fe^{56} X-rays illuminating the back surface were smeared over large numbers of pixels. Work on this problem is on-going, and will be discussed more fully in our reports of our advanced HRI detector contract NASW-3000.

07 08 80 (2) REC



100 mV/div

07 08 80 (1)



07 08 80 (3) Blue

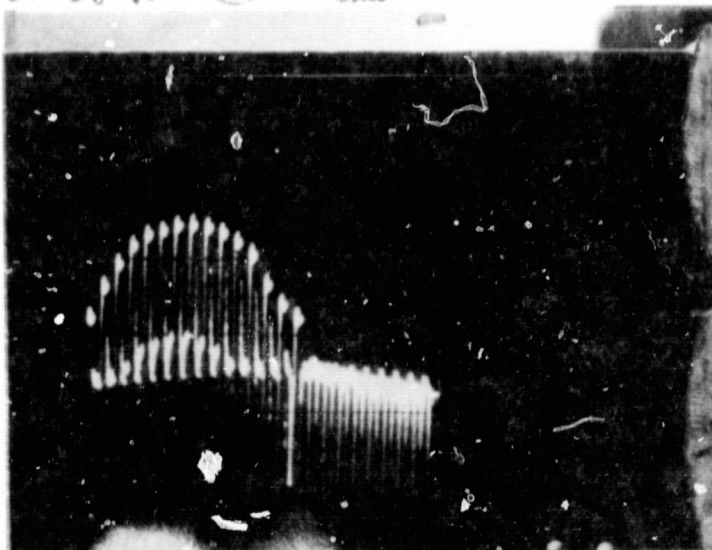


Figure 16. Stand-alone operation of the Westinghouse 100 x 200 chip, backside illuminated. The oscilloscope trace shows that only portions of the chip, behind a circular mask, respond to light.

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3.0 PUBLICATIONS

"Use of a Charge Coupled Device in X-ray Astronomy as a High Resolution Imaging Detector with Spectral Resolution", D.A. Schwartz, R.E. Griffiths, S.S. Murray, M.V. Zombeck, W. Bradley, and J. Barrett, SPIE Proceedings, volume 184, page 247 (1979).

"Area Array X-ray Sensors", D.M. McCann, M.C. Peckerar, W. Mend, D.A. Schwartz, R.E. Griffiths, G. Polucci, and M.V. Zombeck, SPIE Proceedings, volume 217, page 118 (1980).

"Preliminary Results from a Single Photon X-ray Imaging CCD Camera Using a Fairchild CCD 211", R.E. Griffiths, D.A. Schwartz, G. Polucci, S.S. Murray, and M.V. Zombeck, SPIE Proceedings, volume 244, pages 57-65 (1980).

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 15. McCann, D., Peckerar, M., Mend, W., Schwartz, D.A., Griffiths, R.E., Polucci, G., and Zombeck, M.V. 1980, in "Advanced in Focal Plane Technology", SPIE Proceedings, volume 217, page 118.